UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,714	03/23/2001	Satoshi Kamiya	017446/0310	4370

22428 7590 05/05/2005		EXAMINER
FOLEY AND LARDNER SUITE 500 3000 K STREET NW WASHINGTON, DC 20007		RYMAN, DANIEL J

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

	Application No.	**Applicant(s)**
Office Action Summary	09/814,714	KAMIYA, SATOSHI
	Examiner	**Art Unit**
	Daniel J. Ryman	2665

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2001*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☒ All   b)☐ Some * c)☐ None of:

  1.☒ Certified copies of the priority documents have been received.

  2.☐ Certified copies of the priority documents have been received in Application No. _____.

  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1.   Figures 9-13 should be designated by a legend such as --Prior Art-- because only that

which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in

reply to the Office action to avoid abandonment of the application. The replacement sheet(s)

should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to

obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office

action. The objection to the drawings will not be held in abeyance.

2.   The drawings are objected to because in Fig. 6 the processing sequence comprising IM1,

IM2, IM3, and IM4 should be boxed for TS17, TS18, and TS19 in a fashion similar to that for

the processing sequences for the other time slots. Corrected drawing sheets are required in reply

to the Office action to avoid abandonment of the application. Any amended replacement

drawing sheet should include all of the figures appearing on the immediate prior version of the

sheet, even if only one figure is being amended. The figure or figure number of an amended

drawing should not be labeled as "amended." If a drawing figure is to be canceled, the

appropriate figure must be removed from the replacement sheet, and where necessary, the

remaining figures must be renumbered and appropriate changes made to the brief description of

the several views of the drawings for consistency. Additional replacement sheets may be

necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be

labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any

portion of the drawing figures. If the changes are not accepted by the examiner, the applicant

will be notified and informed of any required corrective action in the next Office action. The

objection to the drawings will not be held in abeyance.

Specification

3.   The disclosure is objected to because of the following informalities: on page 4, line 26

"10-1 to 0-4" should be "10-1 to 10-4"; on page 7, line 15 "umber" should be "number"; and on

page 10, lines 12-14 the acronym LSI should be defined.

Appropriate correction is required.

Claim Objections

4.   Claim 4 is objected to because of the following informalities: claim 4 states that each

input module comprises output port reservation information receiving sections, allocators, and

output port reservation information transmitting sections where the output port reservation

information receiving sections, allocators, and output port reservation information transmitting

sections simultaneously execute processing for different reservation time slots. It is unclear from

this limitation if the output port reservation information receiving sections, allocators, and output

port reservation information transmitting sections of each input module simultaneously execute

processing for different reservation time slots within each input module or between the input

modules. Since having each input module simultaneously execute processing for different

reservation time slots is prior art as admitted by Applicant, Examiner will interpret "wherein said

output port reservation information receiving sections, allocators, and output port reservation

information transmitting sections simultaneously execute" to be "wherein said output port

reservation information receiving sections, allocators, and output port reservation information

transmitting sections within each input module simultaneously execute" for prior art rejections.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's

Admitted Prior Art (AAPA) in view of Chao et al. (USPN 5,724,351) in further view of Hanaki

(USPN 6,269,439).

7.   Regarding claim 1, Applicant admits as prior art a distributed pipeline scheduling method

for a system which includes a plurality of input ports for inputting data (Fig. 8 and page 1, line

14-page 4, line 21), a plurality of output ports for outputting data (Fig. 8 and page 1, line 14-page

4, line 21), a data switch element for switching the data input from the input ports and

transferring the data to the output ports (Fig. 8 and page 1, line 14-page 4, line 21), and a

scheduler having a distributed scheduling architecture for controlling the data switch element

(Figs. 8 and 9 and page 1, line 14-page 5, line 24), and determines connection reservations

between the input ports and the output ports (Figs. 8 and 9 and page 1, line 14-page 5, line 24),

comprising the steps of: causing the scheduler to assign time slots to information transfer

processing and reservation processing (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and

page 8, line 17-page 10, line 14); and processing information transfer processing and reservation

processing in the assigned time slots (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page

8, line 17-page 10, line 14).

Applicant does not admit as prior art causing the scheduler to independently assign time

slots to information transfer processing and reservation processing; and processing information

transfer processing and reservation processing in the assigned time slots in a pipeline fashion.

Rather Applicant admits as prior art that the scheduler assigns the same time slot to information

transfer processing and reservation processing (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24;

and page 8, line 17-page 10, line 14). Chao teaches, in a packet switching system, that adequate

performance of a large switch is only possible by using pipeline techniques in the scheduler

(arbiter) (col. 6, lines 27-37); however, Chao does not specify how the pipeline processing is

performed. Thus, it would have been obvious to one of ordinary skill in the art at the time of the

invention to process information transfer processing and reservation processing in assigned time

slots in a pipeline fashion in order to have adequate performance in a large switch.

Applicant in view of Chao does not expressly disclose that the scheduler independently

assigns time slots to information transfer processing and reservation processing; however,

Applicant in view of Chao does disclose performing pipeline processing in the scheduler (Chao:

col. 6, lines 27-37) where the scheduler performs information transfer processing and reservation

processing (AAPA: Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page

10, line 14). Hanaki teaches, in a pipeline processing system, independently assigning time slots

to different stages of the pipeline processor in order to increase the amount of processing that can

be accomplished per unit time compared to a processor without pipeline processing (Fig. 2 and

col. 1, lines 42-67). Thus, it would have been obvious to one of ordinary skill in the art at the

time of the invention to independently assign time slots to information transfer processing and

reservation processing in order to increase the amount of processing that can be accomplished

per unit time compared to a processor without pipeline processing.

8.   Regarding claim 2, Applicant in view of Chao in further view of Hanaki discloses that the

scheduler includes N (N is a natural number) distributed scheduling modules for performing

information transfer processing and reservation processing in units of time slots (AAPA: Figs. 8

and 9 and page 1, line 14-page 5, line 24), and the step of processing comprises the step of

determining a connection reservation, by using the distributed scheduling module, for a

predetermined time slot at a time point after a lapse of a time corresponding to a number time

slots from a time slot from which the reservation processing is started (AAPA: Figs. 8 and 9 and

page 1, line 14-page 5, line 24; Chao: col. 6, lines 27-37; and Hanaki: Fig. 2 and col. 1, lines 42-

67). Applicant in view of Chao in further view of Hanaki does not expressly disclose that the

number of time slots is 2N-1 time slots; however, Applicant in view of Chao in further view of

Hanaki does disclose that there is a number of time slots between the start of the processing and

the predetermined time slot which is being reserved (AAPA: Figs. 8 and 9 and page 1, line 14-

page 5, line 24; Chao: col. 6, lines 27-37; and Hanaki: Fig. 2 and col. 1, lines 42-67). It is

generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize

the numerical parameters or values of any system absent a showing of criticality in a particular

recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32

USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471

(1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454,

105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re

Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215

(CCPA 1980). Since Applicant in view of Chao in further view of Hanaki discloses that there is

a number of time slots between the start of the processing and the predetermined time slot which

is being reserved, it would have been obvious at the time of the invention to use any number of

time slots, including 2N-1, absent a showing of criticality by Applicant.

9.   Regarding claim 3, Applicant admits as prior art a distributed pipeline scheduling system

comprising a plurality of input ports for inputting data (Fig. 8 and page 1, line 14-page 4, line

21), a plurality of output ports for outputting data (Fig. 8 and page 1, line 14-page 4, line 21), a

data switch element for switching the data input from the input ports and transferring the data to

the output ports (Fig. 8 and page 1, line 14-page 4, line 21), and a scheduler having a distributed

scheduling architecture for controlling the data switch element (Figs. 8 and 9 and page 1, line 14-

page 5, line 24), wherein said scheduler comprises a plurality of input modules for performing

reservation processing for different time slots (Figs. 8, 9, and 13; page 1, line 14-page 10, line

14), and said input modules respectively comprise information transfer processing means and

reservation processing means for performing information transfer and reservation processing for

different time slots (Figs. 8, 9, and 13; page 1, line 14-page 10, line 14).

Applicant does not admit as prior art that the scheduler comprises a plurality of input

modules for performing reservation processing for different time slots at the same time in a

pipeline fashion, and the input modules respectively comprise information transfer processing

means and reservation processing means for performing information transfer and reservation

processing for different time slots at the same time in a pipeline fashion. Chao teaches, in a

packet switching system, that adequate performance of a large switch is only possible by using

pipeline techniques in the scheduler (arbiter) (col. 6, lines 27-37); however, Chao does not

specify how the pipeline processing is performed. Thus, it would have been obvious to one of

ordinary skill in the art at the time of the invention to have the scheduler comprise a plurality of

input modules for performing reservation processing in a pipeline fashion and to have the input

modules respectively comprise information transfer processing means and reservation processing

means for performing information transfer and reservation processing in a pipeline fashion in

order to have adequate performance in a large switch.

Applicant in view of Chao does not expressly disclose that that the scheduler comprises a

plurality of input modules for performing reservation processing for different time slots at the

same time, and said input modules respectively comprise information transfer processing means

and reservation processing means for performing information transfer and reservation processing

for different time slots at the same time; however, Applicant in view of Chao does disclose

performing pipeline processing in the scheduler (Chao: col. 6, lines 27-37) where the scheduler

performs information transfer processing and reservation processing (AAPA: Figs. 8, 9, and 13;

page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14). Hanaki teaches, in a

pipeline processing system, independently assigning time slots to different stages of the pipeline

processor in order to increase the amount of processing that can be accomplished per unit time

compared to a processor without pipeline processing (Fig. 2 and col. 1, lines 42-67). Thus, it

would have been obvious to one of ordinary skill in the art at the time of the invention to have

the scheduler comprise a plurality of input modules for performing reservation processing for

different time slots at the same time in a pipeline fashion, and said input modules respectively

comprise information transfer processing means and reservation processing means for

performing information transfer and reservation processing for different time slots at the same

time in a pipeline fashion in order to increase the amount of processing that can be accomplished

per unit time compared to a processor without pipeline processing.

10.   Regarding claim 4, Applicant admits as prior art a distributed scheduler for distributed

pipeline scheduling which is used by a packet switch in a packet switching system (Fig. 8 and

page 1, line 14-page 4, line 21), comprising: a plurality of input modules respectively having

output port reservation information receiving sections, allocators, and output port reservation

information transmitting sections and serving to perform distributed scheduling (Figs. 8, 9, and

13 and page 1, line 14-page 10, line 14), wherein said output port reservation information

receiving sections, allocators, and output port reservation information transmitting sections

execute processing for different reservation time slots (Figs. 8, 9, and 13; page 1, line 14-page 5,

line 24; and page 8, line 17-page 10, line 14).

Applicant does not admit as prior art that the output port reservation information

receiving sections, allocators, and output port reservation information transmitting sections

within each input module simultaneously execute processing for different reservation time slots.

Chao teaches, in a packet switching system, that adequate performance of a large switch is only

possible by using pipeline techniques in the scheduler (arbiter) (col. 6, lines 27-37); however,

Chao does not specify how the pipeline processing is performed. Thus, it would have been

obvious to one of ordinary skill in the art at the time of the invention to perform pipeline

processing in each input module in order to have adequate performance in a large switch.

Applicant in view of Chao does not expressly disclose that the output port reservation

information receiving sections, allocators, and output port reservation information transmitting

sections within each input module simultaneously execute processing for different reservation

time slots. Hanaki teaches, in a pipeline processing system, simultaneously execute processing

for different items in the elements of a pipeline processor in order to increase the amount of

processing that can be accomplished per unit time compared to a processor without pipeline

processing (Fig. 2 and col. 1, lines 42-67). Thus, it would have been obvious to one of ordinary

skill in the art at the time of the invention to have the output port reservation information

receiving sections, allocators, and output port reservation information transmitting sections

within each input module simultaneously execute processing for different reservation time slots

in order to increase the amount of processing that can be accomplished per unit time compared to

a processor without pipeline processing.

Conclusion

11.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure. Jordan et al. (USPN 5,805,849) see col. 1, lines 52-67 which pertain to the benefits of

pipelined processors. Kumar (USPN 6,122,274) see entire document which pertains to a

decentralized pipeline control for a switch.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The

examiner can normally be reached on Mon.-Fri. 7:00-4:30 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

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Daniel J. Ryman
Examiner
Art Unit 2665

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600